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 Katopis, G.A.; Becker, W.D.; Harrer, H.H.;
[Advanced Packaging IEEE Transactions on \[see also Components, Packaging and Manufacturing Technology, Part B: Advanced Packaging IEEE Transactions on\]](#)
 Volume 28, Issue 1, Feb 2005 Page(s):24 - 31
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 Swift, S.;
[OCEANS](#)
 Volume 15, Aug 1983 Page(s):150 - 154
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[WESCON/98](#)
 15-17 Sept. 1998 Page(s):315 - 320
 Digital Object Identifier 10.1109/WESCON.1998.716474
[AbstractPlus](#) | Full Text: [PDF](#)(484 KB) [IEEE CNF](#)
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- ☐ 6. **A microprocessor with a 128-bit CPU, ten floating-point MAC's, four floating-point dividers, and an MPEG-2**

decoder

Suzuoki, M.; Kutaragi, K.; Hiroi, T.; Magoshi, H.; Okamoto, S.; Oka, M.; Ohba, A.; Yamamoto, Y.; Furuhashi, M.; Tanaka, M.; Yutaka, T.; Okada, T.; Nagamatsu, M.; Urakawa, Y.; Funyu, M.; Kunimatsu, A.; Goto, H.; Hashimoto, K.; Ide, N.; Murakami, H.; Ohtaguro, Y.; Aono, A.;
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Abstract

Digital has announced and shipped this first-generation, high-performance network for clusters, the **Memory Channel** for PCI network, and all SMP AlphaServers running Digital Unix support it. Digital has publicly demonstrated **Memory Channel**-connected systems running Windows/NT. The **Memory Channel** network does not require functionality beyond the **PCI bus** specification and works with any system having a **PCI I/O slot**. Production **Memory Channel** clusters can be as large as eight nodes (limited only by first-generation hardware) of 12 processors each (96 processors). One such cluster installed at Supercomputing 95 ran clusterwide applications using High Performance Fortran, PVM, and MPI. A four-node, 48 processor **Memory Channel** cluster, using Oracle Parallel Server, has held the record for TPC-C benchmarks since its introduction in April 1996. The same **Memory Channel** network used to connect this high-end database configuration also cost-effectively supports configuration of two-node, single-processor clusters. Latency over **Memory Channel** for a one-way, user-process-to-user-process message is 2.9 microseconds. The processor overhead is less than 150 ns for a 32-byte message. Standard message-passing APIs benefit greatly from this underlying capability.

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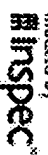
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